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# Advantages and Accuracy of Simulation Tools For Printed Circuit Board Simulation

Shahana Aziz Pagen*
*NASA Goddard Space Flight Center/MEI Technologies, Greenbelt, MD 20771*

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**Up front signal integrity analysis at the module level is becoming more and more critical due to the increasing operating frequencies of digital circuits, faster edge rates, etc. Currently the NASA Goddard Space Flight Center is incorporating the use of Simulation Based SI analysis into the module design flow on the James Webb Space Telescope project. The hardware design team is using simulation tools to guarantee board performance before building all flight hardware. This paper documents the methodology used and includes examples of the simulation results.**

## I. Introduction: Why Simulate?

SIGNAL Integrity (SI) simulation is becoming more common with the availability of quality tools that fit seamlessly into the printed wiring board (PWB) layout flow. SI simulation is becoming increasingly critical due to the faster operational speeds and the newer technology families with faster edge rates and stronger output drive.

Fast edge rates have made it imperative to consider transmission line effects and possible signal integrity problems early in the PWB design phase. Simulation tools make it possible to determine these problems in advance and find the solutions before fabricating hardware, thus eliminating costly re-spins or difficult and cumbersome lab work-arounds.

Signal integrity problems such as overshoot, undershoot, ringing, crosstalk, as well as power and ground integrity problems such as ground bounce and ripple can be modeled, reduced or eliminated, ensuring proper hardware performance. This improves the quality and reliability of the hardware system and enables projects to meet their cost and schedule objectives.

## II. Advanced Simulation Tools

In the module design flow, SI simulation fits into the board layout phase. Simulation tools can be used for both pre and post route simulation. Pre route simulation is used to aid in the selection of device drivers, to determine the placement of critical components, to verify the effectiveness of the printed circuit board (PCB) stack up structure, and to define routing guidelines for critical signal nets.

Post route simulation can be used to validate the completed signal routing and to detect and mitigate potential signal integrity problems. Through the use of simulation tools, solutions to various problems can be found in the form of routing changes, optimized termination schemes, appropriate termination values for the given driver type and load, proper input/output driver selection, decoupling capacitor selection and placement. These changes can be incorporated before the PWB is released to fabrication. This guarantees first pass success with hardware functioning as designed from the moment power is applied.

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*Shahana Pagen is currently working at the NASA Goddard Space Flight Center as the Hardware Development Lead for the James Webb Space Telescope program's Integrated Science Instrument Module Command and Data Handling (ICDH) Subsystem.

In addition to single PCB simulation, these tools also provide the capability to perform multi-board level system simulation. This allows an engineer to model a backplane design with different plug-in card loading effects or module to cable interface characteristics. Multi-board simulation provides an integrated environment to model and guarantee end to end system performance.

In this paper simulations were completed using Mentor Graphics Interconnectix Synthesis (IS)[2] and Sigrity Inc.'s Speed2000[3] simulation tools.

## III. Simulation Models: A Look At Ibis

Simulation tools make use of various model types. The currently available tools use both Spice and IBIS models. IBIS, which is the acronym for Input/Output Buffer Information Specification, is a newer modeling standard that provides a simple table based buffer model for semiconductor devices. IBIS uses non proprietary I-V (current versus voltage) information tables to describe IO buffer behavior. Due to the non proprietary nature on IBIS models, these models are more readily available from semiconductor vendors. IBIS models simulate much faster than Spice models, making them easier to use in a simulation environment to get faster results and run multiple simulation cases.

Figure 1 shows the basic structure of an IBIS Model which contains the following five elements:

1. Pull-down translator
2. Pull-up translator
3. Ground and power clamp diodes
4. Ramp characteristic
5. Package parasitics

The elements of an IBIS model are described below:

1. Pull-down translator
   a. Describes the I/V characteristics during pull-down.
   b. The data is taken for minimum and maximum current for given voltages.
   c. The data ranges from $-$VCC to 2VCC as that allows a behavioral model for signal reflections caused by improper termination and overshoot and undershoot situations when the protection diodes are forward biased.
2. Pull-up translator
   a. Describes the pull-up state of the buffer when the output drives high.
   b. The data for this curve is entered using the formula Vtable $=$ VCC $-$ Voutput
   c. The minimum and maximum values are determined by the minimum and maximum operating temperatures, supply voltages and process variations.

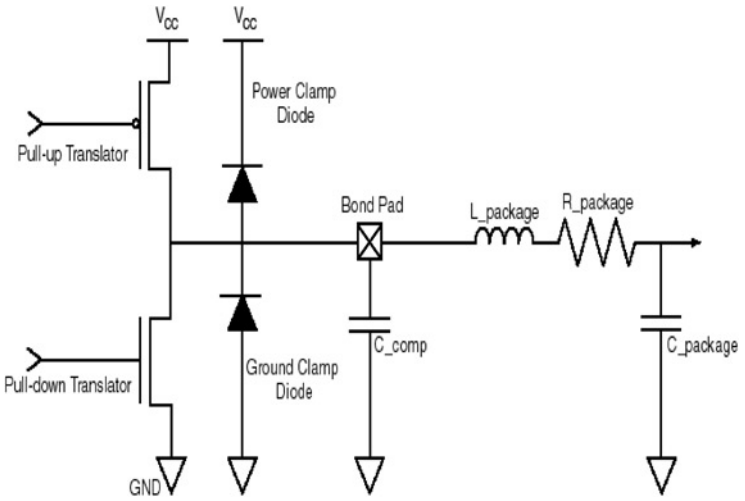


**Fig. 1 Anatomy of an IBIS model.**

   d. Combining the highest current values with the fastest ramp time and minimum package characteristics, a fast model can be derived. A slow model can be derived by combining the lowest current with the slowest ramp time and maximum package characteristics.
3. GND and Power clamp diodes
   a. Describes the ground and power clamp diodes.
   b. The GND clamp curve is derived from the ground relative data gathered while the buffer is in the high-impedance state and illustrates the region where the ground clamp diode is active. The range is from −VCC to VCC.
   c. The power clamp curve is derived from the VCC relative data gathered while the buffer is in a high impedance state and shows the region where the power clamp diode is active. This measurement ranges from VCC to 2VCC.
4. Ramp characteristics
   a. Describes the ramp time for the pull-up and pull-down devices. Ensures proper AC operation of the model.
   b. The min and max columns represent the minimum and maximum slew rates for the buffers.
   c. The values represent the intrinsic values of the transistors with all package parasitics and external loads removed.
5. Package parasitics
   a. Adds the component and package parasitics.
   b. C_comp is the capacitance of the die itself, excluding the package capacitance.
   c. Package characteristic resistance, inductance and capacitance are added by R_pkg, L_pkg, and C_pkg, respectively.

More information on the IBIS format and its different versions are available at the official IBIS forum website.[1]

## IV. Setting Up The Simulation Environment

What makes today's simulation tools powerful and effective is the fact that they are able to incorporate the actual board information, providing enhanced capability compared to basic line simulation. The tools use the actual board construction and routing information, incorporating all the layers, materials, components, traces and vias into the simulation database. This makes the simulation as close to the real world as possible. Figure 2 shows a board layout view after importing into the tool.

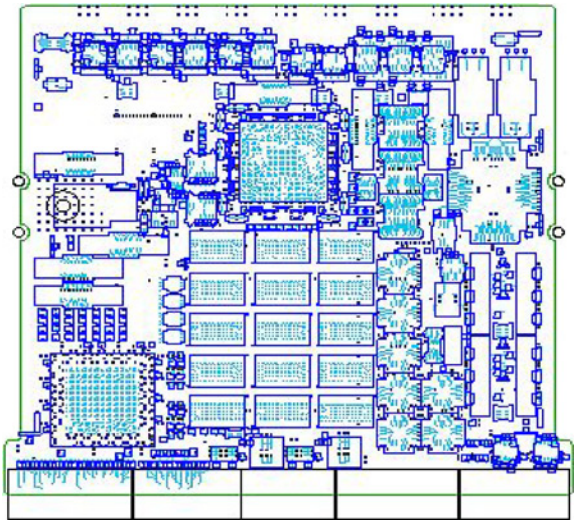

**Fig. 2 Importing the board CAD info into the simulation environment.**

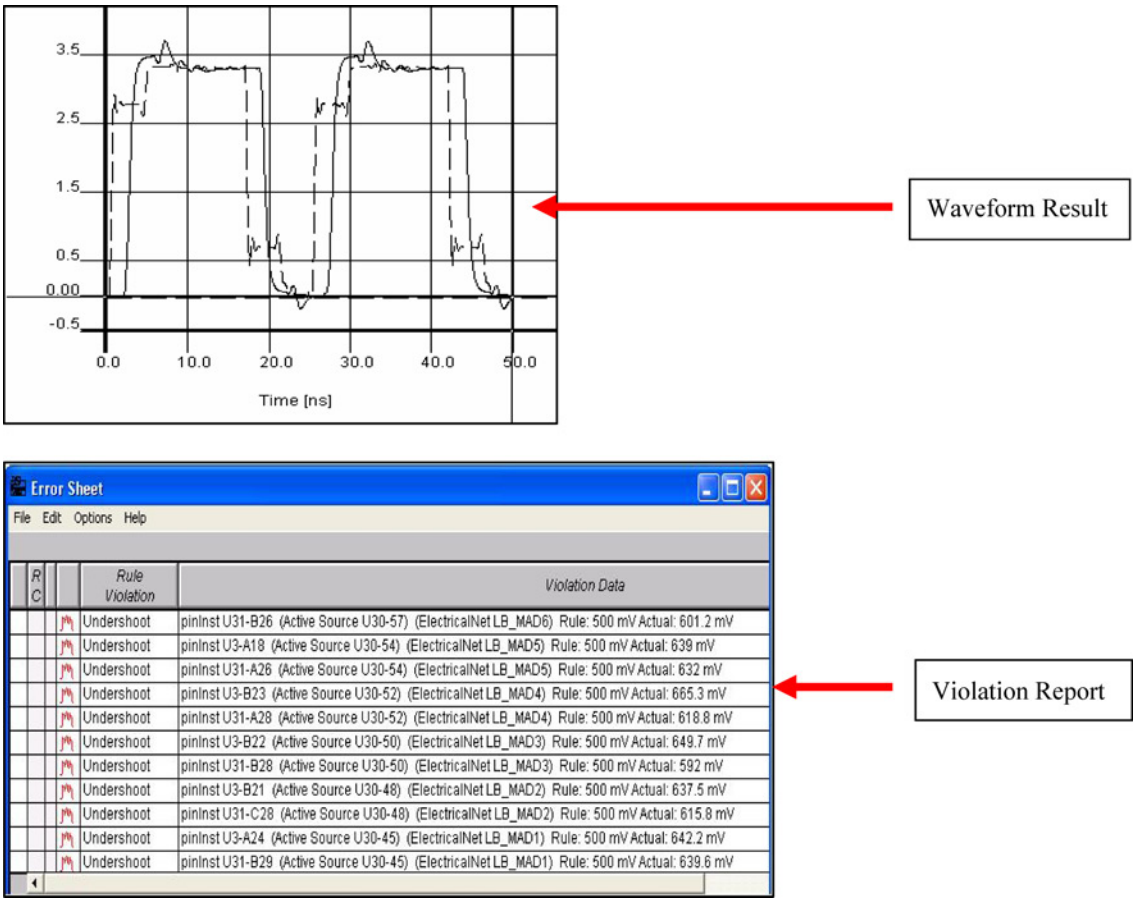


**Fig. 3 Various simulation result options.**

The following steps must be performed to setup a typical simulation database:

1. The engineer must first import the board data into the simulation tool, incorporating the board geometries, materials, layer and routing information.
2. Next the engineer must setup the simulation environment by creating the appropriate stimulus types. The stimulus describes the signal switching frequencies.
3. The nets must be classified to identify clocks, control, data or static signals.
4. Noise rules such as undershoot, overshoot, ringing, crosstalk or required parameters such as characteristic impedance, and timing margins must be specified
5. Finally the device models must be loaded to provide IO information for all switching devices. This completes the simulation setup.

Simulation results are available to the user in both waveform or report format. Figure 3 shows an example of both a waveform result and a crosstalk violation report obtained from the tool.

## V. Simulation Examples

### A. Example 1: Termination Selection and Skew Measurement

Simulation tools are useful in selecting the proper termination topology and value given the driver and receiver type, required switching frequency and noise requirements. The waveform in Fig. 4 shows the simulation of a clock signal at the destination device pin.

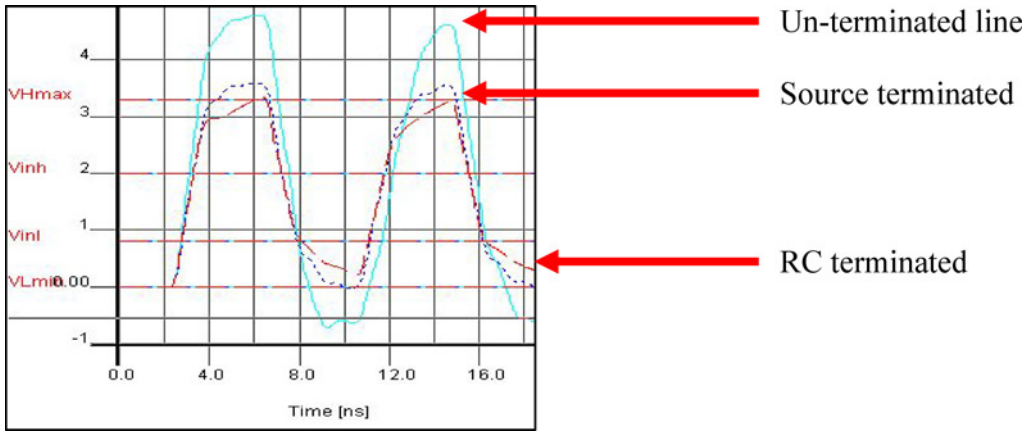


**Fig. 4 Termination strategies.**

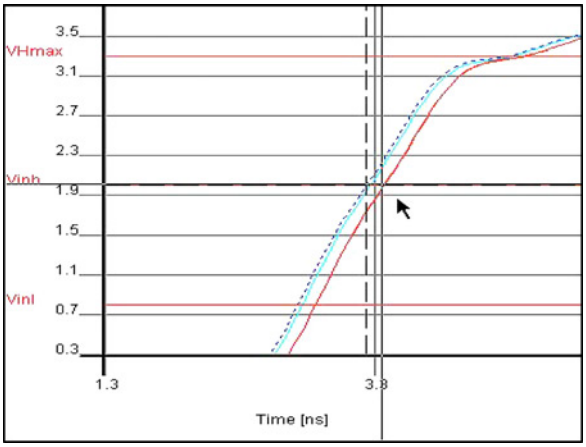


**Fig. 5 Measuring skew.**

Simulation revealed the following:

- Without termination the signal has overshoot and undershoot beyond the device allowed specifications.
- Using an RC termination placed near the destination pin eliminates the overshoot and undershoot, however the RC effects slow the edge such that it does not reach zero volts completely during the high to low transition.
- A 33 Ohm series terminating resistor placed at the driver output pin eliminates the overshoot and undershoot problem and also allows for proper rise and fall times for the signal - making it the solution of choice.

In addition to selecting termination, simulation can be used to determine the skew between different signals as shown in Fig. 5. Simulation waveforms of signals arriving at different destinations can be analyzed to see if the skew between them is acceptable. This makes it possible to measure the delay from source to destination, giving exact board timing numbers that can be incorporated into timing budget calculations.

### B. Example 2: What-if Exploration

This example illustrates another powerful capability of advanced simulation tools – what-if exploration. This gives engineers the ability to compare different operational scenarios within a simulation environment without requiring expensive hardware modifications. This method can be used to test various drivers/receiver types determine the optimum devices for a given source-load configuration.

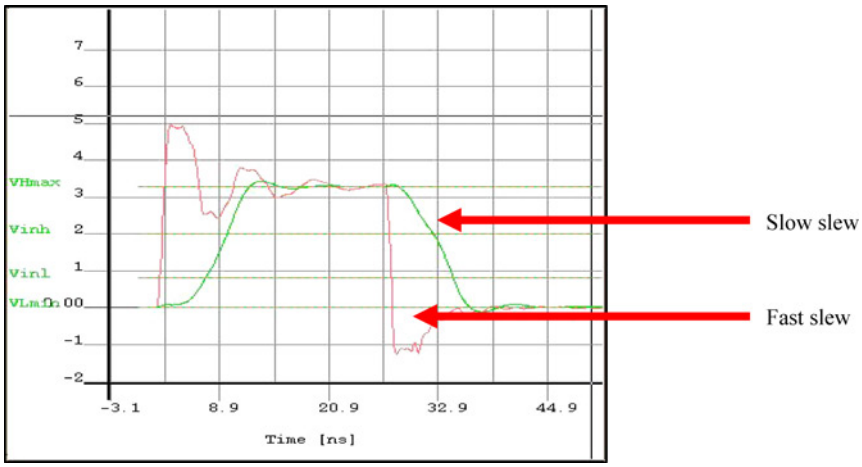


**Fig. 6 AX output driver.**

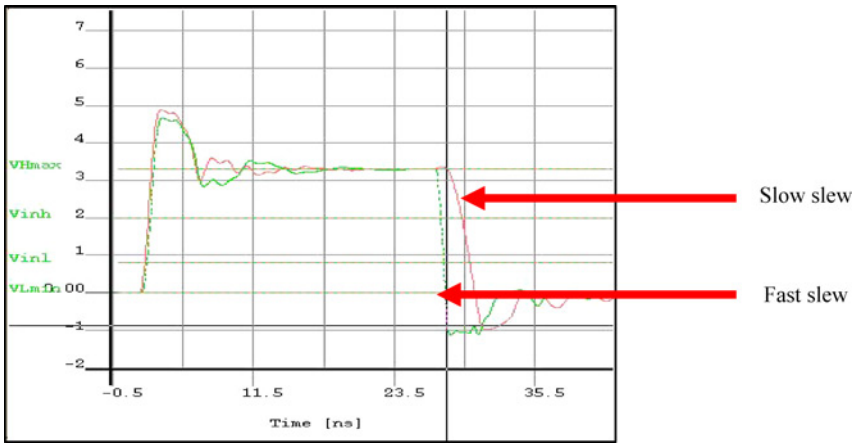


**Fig. 7 SX-S output driver.**

In this example what-if exploration was performed using the Actel[4] Axcelerator (AX) and SX-S family of devices. Since these programmable devices come with different input/output buffer drive options; both the fast and slow slew driver types were used in simulation to determine which option gave the optimum performance to meet both signal integrity and timing constraints.

Simulation showed that:

- The AX fast slew driver violates device abs max specs
- The AX slow slew driver cannot meet output timing though SI is maintained
- The SX-S fast and slow slew driver have same rising edge, slew control only effects the falling edge
- SI still a problem with SX-S regardless of slew

Figure 6 shows the AX driver simulation using both its fast and slow slew drivers whereas Fig. 7 is the simulation waveform with the SX-S family driver.

Simulation further showed that the solution that meets all design constraints is fast slew (of either device) with 45 Ohm series termination. This provides a design constraint to the board designer (termination scheme and value) as well as to the FPGA (field programmable gate array) designer (device and IO type). Figure 8 shows the simulated waveform of the solution to the problem.

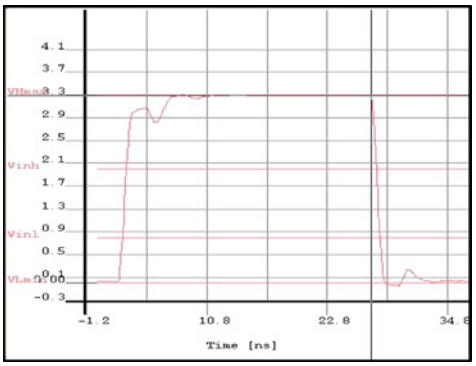


**Fig. 8 SI solution.**

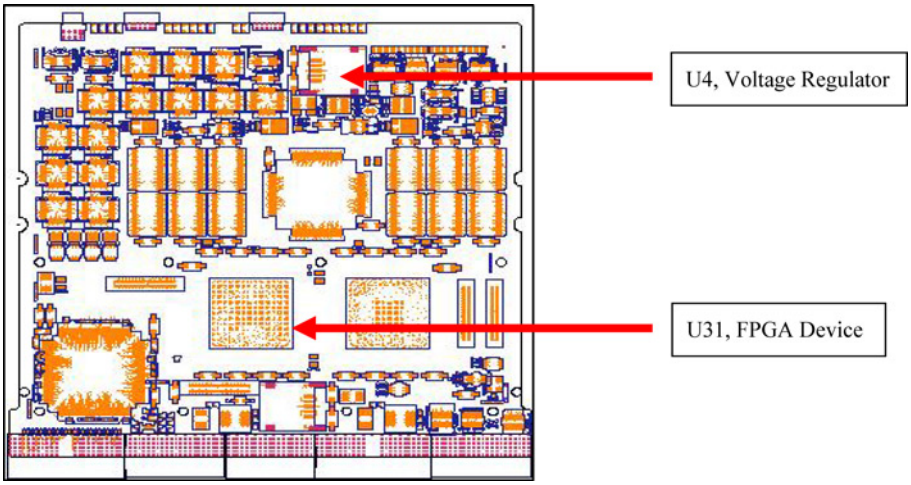


**Fig. 9 Board setup for decoupling capacitor effectiveness simulation.**

### C. Example 3: Decoupling Capacitor Effectiveness and Low Impedance Power Delivery

The third simulation example analyzes the problem of ensuring proper power delivery on a complex circuit board. With devices utilizing large pin count packages, large number of simultaneously switching outputs (SSO) and ever increasing switching speeds—this problem becomes more challenging. Using the "rule of thumb" guidelines for decoupling is no longer sufficient.

In this case, simulation was used to determine the effectiveness of various decoupling strategies so that tradeoffs could be made in selecting the proper values and placement of decoupling capacitors to ensure a low impedance power delivery path.

The input impedance of the FPGA supply voltage delivery path was analyzed using three types of decoupling capacitor arrangements. The FPGA supply voltage regulator is located at U4 and the FPGA is U31. Figure 9 shows the location of both U4 and U31 in the printed circuit board layout.

In the 1st simulation case no decoupling capacitors were used. Simulations showed a resonance at low frequencies (70 MHz). The 2nd simulation used decoupling capacitors and showed that the resonance is much reduced, and the 1st significant spike does not appear until about 800 MHz. In order to demonstrate the tool's what-if exploration capability further, 8 additional capacitors with low ESR at 800 MHz were placed on the board, and with this modification it is seen that the resonance at 800 MHz is even further reduced. The curves are shown in Fig. 10. Based on system requirements, the optimum bypass capacitor value selection and placement can be fine tuned using this simulation technique.

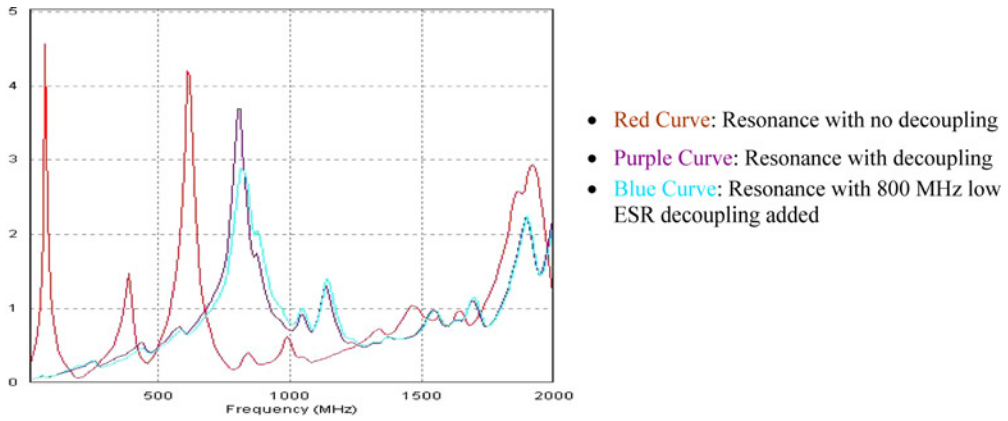


**Fig. 10 Analyzing input impedance of the voltage delivery path.**

### D. Example 4: Effects of Simultaneous Switching Outputs (SSO)

Simulation tools are also capable of analyzing the effects of simultaneous switching outputs or SSO. SSO can cause power rails to glitch and signal bits to operate outside of required specifications. This can cause incorrect logic switching.

This example studies the effect of a 32-bit bi directional data bus. Since the bus is bi-directional, simulations were run with either end acting as the source. One end of the bus is driven by an Actel SX-S family FPGA, while the other end is driven by a Xilinx[5] Virtex-II FPGA. The configuration is shown in Fig. 11. A third FPGA is also part of the bus, but is configured as a receiver for this simulation.

The switching behavior of a data bit (Fig. 12) and the effect on the power rail (Fig. 13) was observed during the SSO operation. The results when the Actel is driving the bus are shown in the red waveform whereas the blue waveform is the result when the Xilinx device is the source.

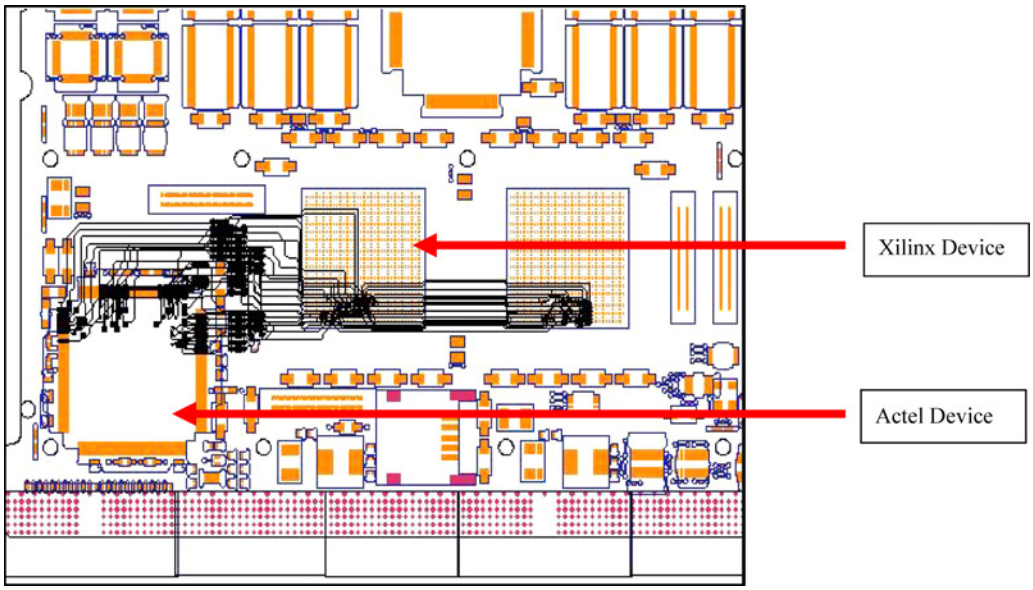


**Fig. 11 Board setup for SSO simulation.**

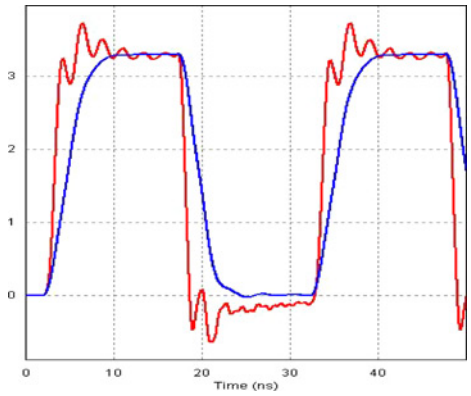


**Fig. 12 SSO effect on data bit.**

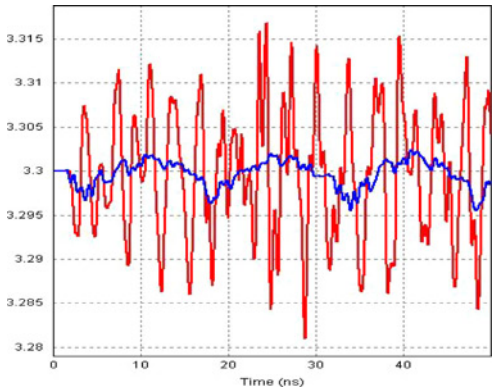


**Fig. 13 SSO effect on power rail.**

As can be seen, the Actel driver causes a higher level of ringing on the data bit and power rail when simultaneously switching the 32 bit bus.

### E. Example 5: Using Simulation Tools for Batch Simulations

Thus far all the examples demonstrated the interactive capabilities of the various simulation tools, where the results were viewed in the waveform format. However, the tools also provide the ability to run a full board analysis constrained by a set of noise rules which generates an output report. The design engineer can then review the violation reports for the entire board and quickly determine the problem areas that may need further attention. This is extremely useful in identifying problem areas that may have crosstalk problems or determining timing numbers for important interfaces. Batch simulations can also check an entire PWB for undershoot/overshoot violations, verifying characteristic impedance values and ringback margins etc.

Figure 14 shows a crosstalk violation summary report identifying all victim and aggressor nets on a PCB and the induced crosstalk values.

The problem can be analyzed further by creating a detailed crosstalk report (as shown in Fig. 15). This report shows the individual contribution of each aggressor net towards the total crosstalk value on a signal. This information can used to selectively fix the worst aggressor problem when moving away all aggressors is not practical.

Batch simulations can also be performed to obtain timing analysis results for the entire board. Figure 16 shows a timing report for min and max delay from source to destination of a memory data bit.

| Rule Category | | Rule Violation | Violation Data |
|---|---|---|---|
| | | Crosstalk | Victim Net: SR_DATA0; Aggressors: BF_SPARE23; Rule: 50 mV Actual: 73.1 mV |
| | | Crosstalk | Victim Net: SR_DATA0; Aggressors: BF_SPARE23; Rule: 50 mV Actual: 63.3 mV |
| | | Crosstalk | Victim Net: SR_DATA0; Aggressors: BF_SPARE23; Rule: 50 mV Actual: 53.6 mV |
| | | Crosstalk | Victim Net: SR_DATA22; Aggressors: $19N933; Rule: 50 mV Actual: 94 mV |
| | | Crosstalk | Victim Net: SR_DATA22; Aggressors: $19N933; Rule: 50 mV Actual: 76.5 mV |
| | | Crosstalk | Victim Net: SR_DATA22; Aggressors: $19N933; Rule: 50 mV Actual: 58.2 mV |
| | | Crosstalk | Victim Net: SR_DATA22; Aggressors: $19N933; Rule: 50 mV Actual: 64.9 mV |
| | | Crosstalk | Victim Net: SR_DATA22; Aggressors: $19N933; Rule: 50 mV Actual: 68.7 mV |
| | | Crosstalk | Victim Net: SR_DATA79; Aggressors: LB_SCMD_ACCEPT3 LB_SPARE8 SR_ADD |
| | | Crosstalk | Victim Net: SR_DATA79; Aggressors: LB_SCMD_ACCEPT3 LB_SPARE8 SR_ADD |

**Fig. 14 Crosstalk simulation violation report.**

Name: 3560 Type: Error Save...

```
Noise:
   Error

Rule Violated:
   Crosstalk

Violation Data:
   ;; Crosstalk Error: (3560)
   ;;    pinInst U57-C2
   ;;    crosstalk method: Default
   ;;    Victim Net: SR_BE_N6
   ;;    Driver on victim net: U44-R28
   ;;    Driver State: LogicLow
   ;;    Crosstalk value and its peak time from each aggressor net
   ;;      SR_ADDR_B13  U44-AA26   66.30   34.55
   ;;      SR_ADDR_C5  U44-N26   54.20   34.55
   ;;      SR_DATA34  U44-M34    0.10   12.45
   ;;    Rule: 50 mV   Actual: 120.3 mV
```

**Fig. 15 Crosstalk violation detailed report.**

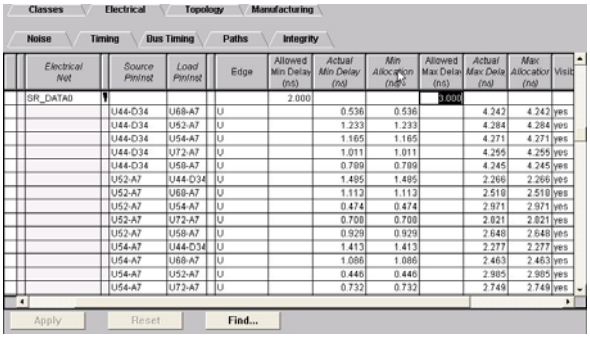


**Fig. 16 Timing analysis report.**

## VI. Determining Simulation Accuracy

Performing complex simulations can only be useful if a direct correlation exists between real world behavior and the simulation results. Proving simulation accuracy is an important part of gaining confidence in the simulation tools, models and results.

To validate the accuracy of simulations, comparison measurements were made wherever possible on fabricated hardware. This is an on-going effort and some of the results are presented in this paper.

### A. Example 1: Comparing Xilinx Output Characteristics

The first comparison was done to validate the Xilinx Virtex-II output models. Measurement was taken of a data bit at the destination device pin. Measurements were taken for both a low to high and a high to low transition.

Figures 17 and 19 are the lab measurements while Figs. 18 and 20 are the simulated waveforms.

The following comparisons were made:

- The voltage high and low value agreed in both simulation and lab measured data to within 100 mV.
- The rise and fall times agreed to within 100 ps.
- General wave shape was similar.

Based on the measurements, it can be concluded that a high degree of correlation exist between the Xilinx models and the actual device behavior.

### B. Example 2: Comparing Multiple Nodes on a Single Trace

Simulation tools offer the ability to view a signal at any point along the trace – not only the destination device pin, but also the source, termination pads (if any) and vias that the signal may traverse through. For this example, comparison measurements were made at three nodes on the same trace.

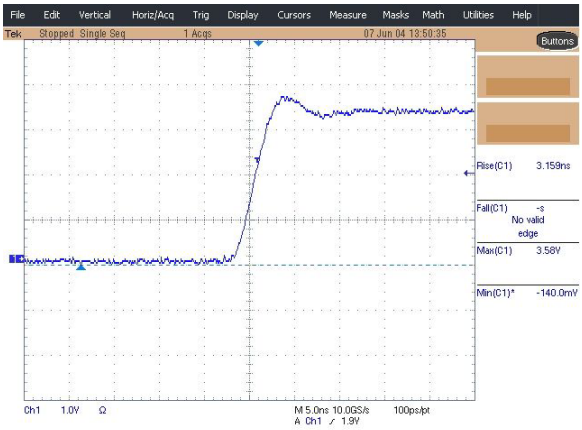


**Fig. 17 Xilinx transition to high output in the lab.**

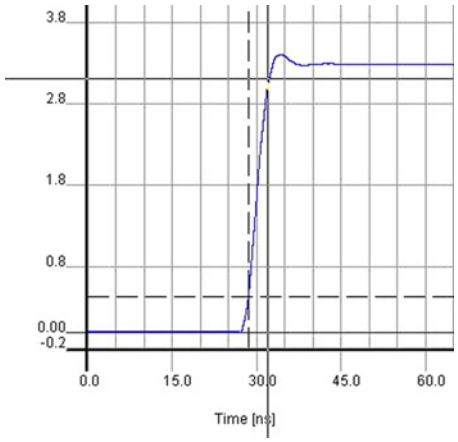


**Fig. 18 Xilinx transition to high output in simulation.**

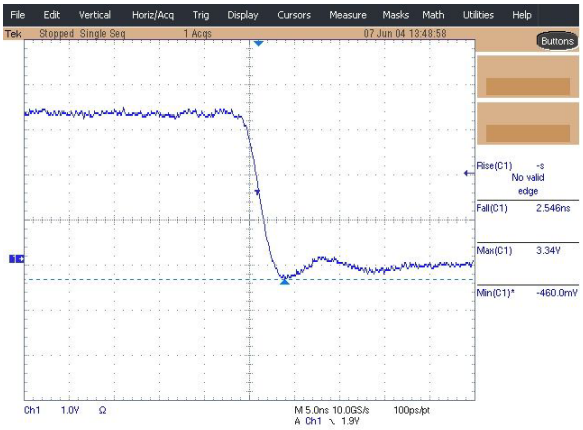


**Fig. 19 Xilinx transition to low output in the lab.**

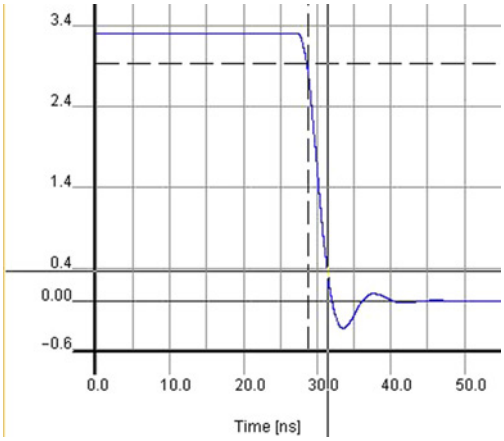


**Fig. 20 Xilinx transition to low output in simulation.**

The three nodes chosen for comparison were:

1. The source output pin
2. The termination resistor node away from the source output pin
3. The destination device pin

In this case the transition to high was observed, and again, it was noted that the high voltage, rise time and general wave shape agreed between both the actual and simulated for all three chosen nodes. Figs. 21 and 22 show the measured and simulated waveform respectively.

### C. Example 3: Comparing Actel Output Characteristics

The third example looks at the Actel AX family output driver. Measurements were taken using the same method as in example 1 comparing the Xilinx output driver.

In this case the following was seen:

- The voltage high and low values agreed fairly closely between simulated and actual
- Rise time in lab measurement was 2.07 ns while in simulation it was .9 ns
- Fall time in lab was 1.485 ns while in simulation was .7 ns
- More ringing was observed in the simulation then in the actual measurement

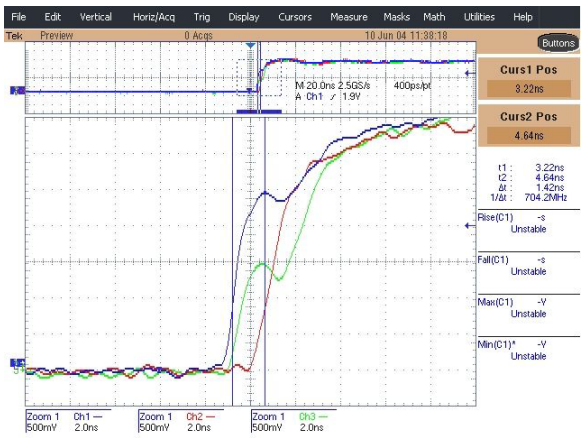


**Fig. 21 Three nodes along the trace as measured in the lab.**

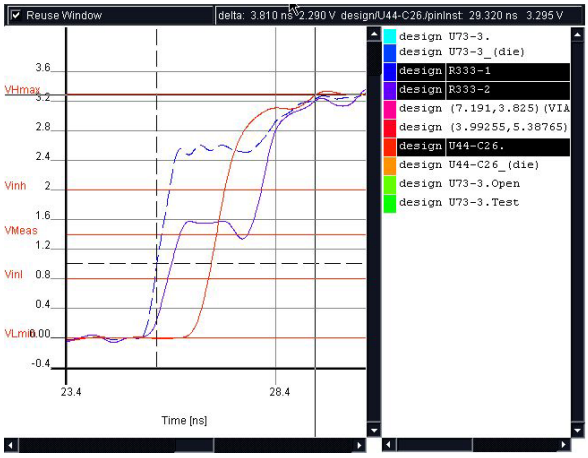


**Fig. 22 Same three nodes in simulation.**

Some possible causes for the mismatch were hypothesized as follows:

- In the simulation environment the FPGA was assumed to be installed directly on the board, on the prototype board the FPGA was installed in a socket. It was hypothesized that the socket parasitics may cause some of the variation, however this was later discounted as an updated simulation was run using the socket RLC in the model and no noticeable difference was seen.
- Using the min current IBIS curve, it is possible to achieve a slower rise and fall time in simulation, which is closer to the actual, so a possibility exists that the typical IBIS curve used in the initial simulation does not completely reflect the device behavior.
- Since Actel AX parts are a new device family, the IBIS models currently available may not be representative of a typical part.

To continue this study further, simulations will be repeated if a newer update of the model becomes available from Actel.

### D. Example 4: Another Look at Actel Drivers

In this final example another comparison was conducted using the Actel AX drivers. Given that the main objective of performing signal integrity simulation is to identify potential problems, this example focuses on the SI problems faced and the solution determined by the tool to mitigate the problem.

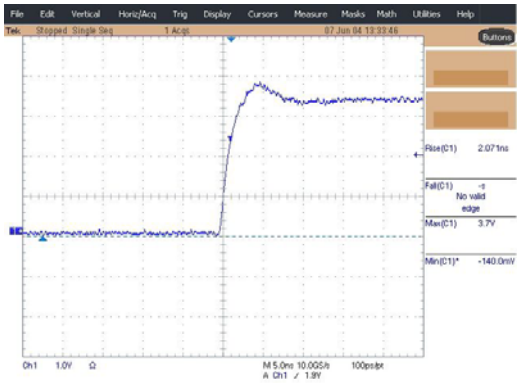


**Fig. 23 Actel transition to high output in the lab.**

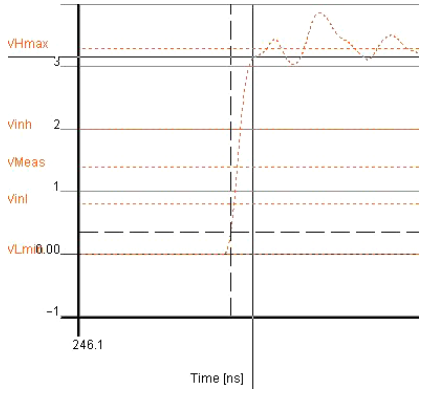


**Fig. 24 Actel transition to high output in simulation.**

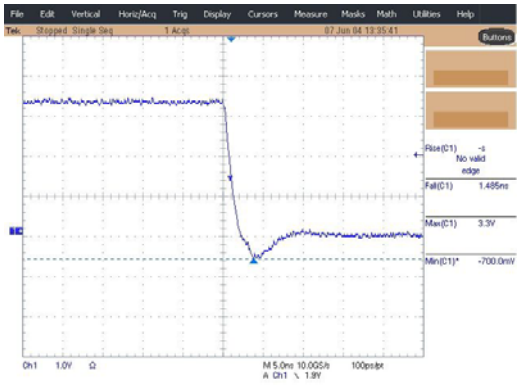


**Fig. 25 Actel transition to low output in the lab.**

Simulations had originally revealed a large magnitude of undershoot that violated the device datasheet specifications. Simulating various termination cases, it was found that without termination, the magnitude of the violation was very large. Figures 23 and 25 show a lab measurement of an Actel output transitioning to high (Fig. 23) and low (Fig. 25), while Figs. 24 and 26 shows an Actel output transitioning to high and low respectively in simulation. This

was improved using a 45 ohm series termination and even further improved (bringing the overshoot and undershoot value to within the device specifications) using a 56 ohm series termination.

To validate the conclusion reached, fabricated hardware (where termination resistors had been installed) was taken and the termination on 2 of the traces was modified. One resistor was replaced with a zero ohm resistor and another was replaced by a 45 ohm resistor and lab measurements were taken.

In all cases, though there is some discrepancy with the actual transition ramp time, the voltage low value agrees fairly closely.

In simulation (as shown in Fig. 27 below):

- Approximately −.9 V undershoot is seen with the 0 ohm resistor
- Approximately −.58 V undershoot is seen with the 45 ohm resistor
- Approximately −.38 V undershoot is seen with the 56 ohm resistor

The lab measurement indicates (Fig. 28):

- Undershoot of −1.1 V with 0 ohm
- −.48 V undershoot with 45 ohm
- −.26 V undershoot with 56 ohm

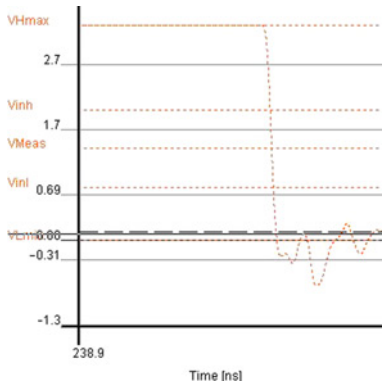


**Fig. 26 Actel transition to low output in simulation.**

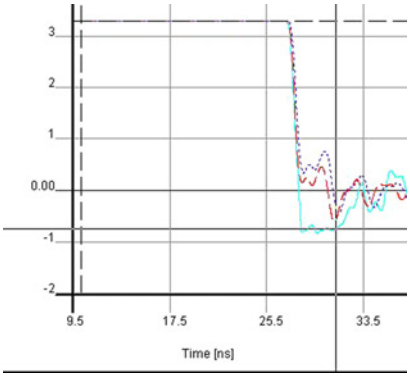


**Fig. 27 Simulations with 0 ohm, 45 ohm and 56 ohm termination.**

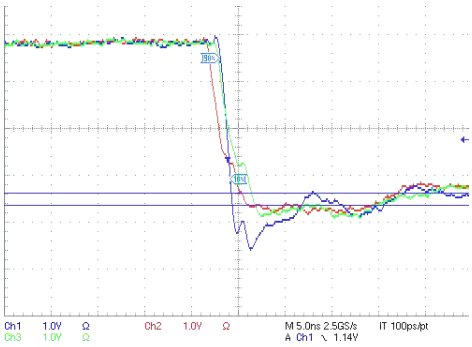


**Fig. 28 Lab measurements with 0 ohm, 45 ohm and 56 ohm termination.**

Thus it is observed that the voltage values agree quite closely and the conclusions reached using simulations were valid. Adding termination was indeed the right choice and the value suggested by the simulation tool to eliminate the undershoot problem was also correct.

## VII. The Future of SI Simulation at NASA

The NASA Goddard Space Flight Center is currently incorporating the use of simulation based SI analysis into the module design flow on the James Webb Space Telescope project.

The Integrated Science Instrument Module Command and Data Handling hardware design team is using simulation tools to guarantee board performance before building hardware and will continue this methodology into the flight board designs. Currently the development units are being delivered and comparison measurements are being made in the lab with each hardware module that becomes available.

## VIII. Conclusion

Simply relying on traditional laboratory based SI analysis for module designs is no longer feasible due to the complexity of the circuit board designs and the changing device technologies. As designs get more complex and device families get faster, simulation tools will give design engineers an extra level of confidence in the hardware that they build and deliver.

## Acknowledgments


- [1]http://www.eigroup.org/ibis/
- [2]http:// www.mentor.com/icx
- [3]http:// www.sigrity.com
- [4]http://www.actel.com
- [5]http:// www.xilinx.com


## Acronyms

| | |
|---|---|
| AX | Axcelerator |
| CAD | Computer Aided Drawing |
| FPGA | Field Programmable Gate Array |
| IBIS | Input/Output Buffer Information Specification |
| ns | Nano-second |
| PCB | Printed Circuit Board |
| PWB | Printed Wiring Board |
| SI | Signal Integrity |
| SSO | Simultaneous Switching Outputs |

Stanley Nissen
*Associate Editor*